Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (previously amended): A semiconductor device, comprising:

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide formed over said P-type region;

a P^+ gate electrode formed over said thick oxide and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent the gate electrode and coupled to a second voltage supply line,

whereby said semiconductor device functions as a capacitor during operation.

Claim 2 (original): The device of claim 1, wherein a gate-to-substrate voltage is maintained at less than zero volts.

Claim 3 (original): The device of claim 1, wherein said P^+ gate comprises polysilicon.

Claim 4 (original): The device of claim 1, wherein said N-type substrate comprises a deep NWELL.

Claim 5 (original): The device of claim 1, wherein said thick oxide is between about 20 and 100 Å thick.

Claim 6 (previously amended): A phase locked loop circuit, comprising:

an oscillator to output a reference clock signal;

a reference frequency divider to receive and divide the reference clock signal, and output a reference signal;

a comparison frequency divider to receive a control voltage signal and output a comparison signal;

a phase comparator to receive the reference signal and the comparison signal, wherein said phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal;

a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal;

a low-pass filter to receive the charge pump signal and output a low pass filter signal; and

a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal,

wherein said low-pass filter comprises a capacitor formed by

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide formed over said P-type region;

a P^+ gate electrode formed over said thick oxide and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent the gate electrode and coupled to a second voltage supply line.

Claim 7 (original): The circuit of claim 6, wherein a gate-to-substrate voltage is maintained at less than zero volts.

Claim 8 (original): The circuit of claim 6, wherein said P^+ gate comprises polysilicon.

Claim 9 (original): The circuit of claim 6, wherein said N-type substrate comprises a deep NWELL.

Claim 10 (original): The circuit of claim 6, wherein said thick oxide is between about 20 and 100 Å thick.

Claim 11 (original): In a low-pass filter for a phase locked loop (PLL) circuit, a capacitor comprising:

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide formed over said P-type region;

a P^+ gate electrode formed over said thick oxide and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent the gate electrode and coupled to a second voltage supply line,

whereby a gate-to-substrate voltage is maintained at less than zero volts to maintain a stable control voltage for the PLL.

Claim 12 (original): The capacitor of claim 11, wherein a gate-to-substrate voltage is maintained at less than zero volts.

Claim 13 (original): The capacitor of claim 11, wherein said P^+ gate electrode comprises polysilicon.

Claim 14 (original): The capacitor of claim 11, wherein said N-type substrate comprises a deep NWELL.

Claim 15 (original): The capacitor of claim 11, wherein said thick oxide is between about 20 and 100 Å thick.

Claim 16 (original): A method of making a semiconductor device, comprising the steps of:

forming a P-type region within an N-type substrate;

forming a thick oxide over said P-type region;

forming a P^+ gate electrode over said thick oxide; and

forming P^+ pick-up terminals within said P-type region adjacent the gate electrode,

whereby coupling the P^+ gate electrode to a first voltage supply line and the P^+ pick-up terminals to a second voltage supply line permits said semiconductor device to function as a capacitor.

Claim 17 (original): The method of claim 16, further comprising the step of forming the P^+ gate electrode of polysilicon.

Claim 18 (original): The method of claim 16, further comprising the step of forming the N-type substrate as a deep NWELL.

Claim 19 (original): The method of claim 16, further comprising the step of forming the thick oxide to a thickness of between about 20 and 100 Å.

Claim 20 (new): A semiconductor device, consisting essentially of:

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide formed over said P-type region;

a P^+ gate electrode formed over said thick oxide and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent the gate electrode and coupled to a second voltage supply line,

whereby said semiconductor device functions as a capacitor during operation.

Claim 21 (new): The device of claim 20, wherein a gate-to-substrate voltage is maintained at less than zero volts.

Claim 22 (new): The device of claim 20, wherein said P^+ gate comprises polysilicon.

Claim 23 (new): The device of claim 20, wherein said N-type substrate comprises a deep NWELL.

Claim 24 (new): The device of claim 20, wherein said thick oxide is between about 20 and 100 Å thick.